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# Pattern Recognition Using Current Mode Hamming Neural Network Circuit

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**Abstract—** *This paper presents 0-9 digits pattern recognition circuit using current-mode hamming neural network. Neural Network is a network which comprises of number of neurons. It works in a similar way as a human brain. There are three layers in Neural Network input layer, hidden layer and output layer. The first layer is template matching calculation subnet in which templates are stored. The second layer is hidden layer in which input patterns compete with each other in order to match with the stored template. The third layer is output layer which provide output according to the corresponding input pattern highly matched with stored pattern. This circuit is implemented at 180 nm technology at 1.8V power supply with input frequency 100MHz. Number of transistors used in this circuit are 460 and average power consumption is 27.2mW.*

## 1. INTRODUCTION

In VLSI technology, as we are succeeding forward, there is requirement of technology which provides precise, predictive and accurate results. Neural Networking plays a vital role to accomplish these requirements [1]. One of its specific applications is pattern recognition in which a particular input pattern is analyzed by the neural network and compared with its stored pattern. Order of degree of matching for stored pattern and input pattern can be determined by using artificial intelligence technology.

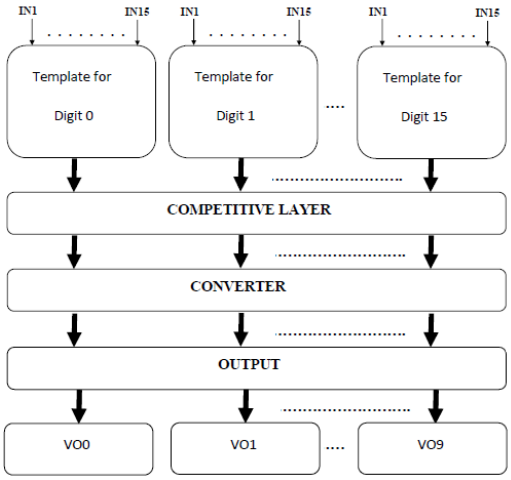


**Fig. 1: Block diagram.**

In this paper 0-9 digit pattern recognition circuit has been implemented using current-mode hamming neural network technology [5]. Basic functioning of implemented pattern recognition circuit is as shown in Fig. 1. Firstly, templates have to be stored in neural networks. Afterwards, a competitive layer is designed according to the number of competing templates. In competitive layer, neuron having highest priority, wins while other neurons inhibit in this phenomenon. By using converter, current corresponding to different templates converts in to their relevant voltage level. Output of highest matching template should have the highest voltage level while all other should be at zero or low level.

## 2. IMPLEMENTATION OF 0-9 DIGITS PATTERN RECOGNITION CIRCUIT.

In current mode hamming neural network, N binary inputs, a template matching and winner take all subnets are provided. Template matching calculation subnet includes M first neurons in which M exemplar templates are stored. Input pattern which highly matched with these stored patterns generates maximum current among all. Winner take all circuit inhibits all other input response except highly matched input.

By using the above concept of current mode hamming neural network, 0-9 digit pattern recognition circuit has been designed. Firstly all decimal digits have to be converted in to the binary bit pattern as shown in table 1.Logic 1 and logic 0 are representing the dark and light portion of pattern respectively as shown in Fig. 3.

For storing 1, input is given at the gate terminal of NMOS while PMOS is used for current steering circuit and vice versa is true for storing 0.

For example storing pattern of binary number 101 is as shown in Fig. 2. Similarly binary pattern for 0 to 9 digits can be stored.

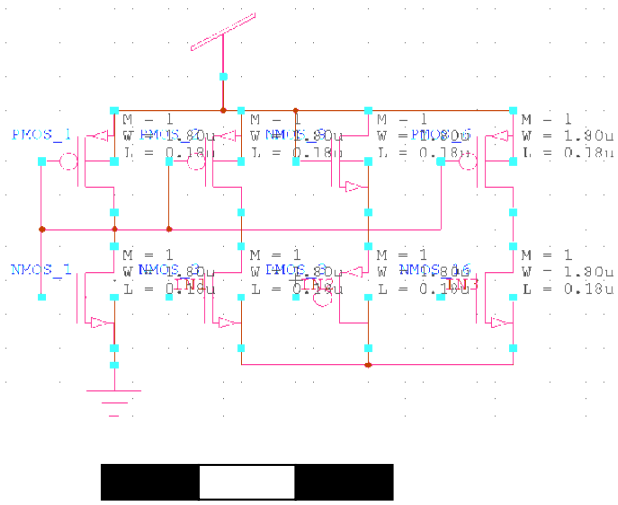

**Fig. 2: Storing pattern for binary number 101.**

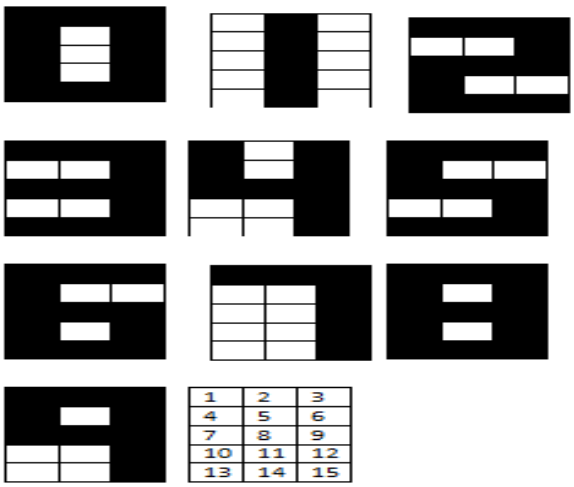


**Fig. 3: Recognizing patterns for the circuit.**

**Table 1: Input pattern corresponding to the digits.**

| Number | Input Pattern |
|---|---|
| 0 | 111 101 101 101 111 |
| 1 | 010 010 010 010 010 |
| 2 | 111 001 111 001 111 |
| 3 | 111 001 111 001 111 |
| 4 | 101 101 111 001 001 |
| 5 | 111 100 111 001 111 |
| 6 | 111 100 111 101 111 |
| 7 | 111 001 001 001 001 |
| 8 | 111 101 111 101 111 |
| 9 | 111 101 111 001 001 |

Table 1 shown above is formed by using the 5*3 matrix shown in Fig. 3.

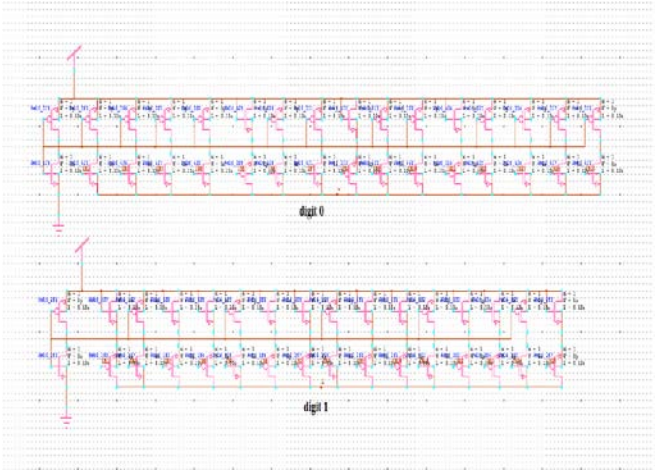


**Fig. 4: Storing pattern for digit 0 and digit 1 corresponding to binary patterns.**

Fig. 4 shows method for storing the digit 0 and digit 1. Connections between NMOS and PMOS are in the same way as shown in Fig. 2. With the similar approach storing templates for 2 to 9 digit can be implemented corresponding to their binary pattern as described in Table 1. In Fig. 3 a matrix of 5*3 is shown for each bit of binary pattern of particular digit. Bit '1' is shown with dark and bit '0' with white box.

Input patterns for 0 to 9 digit binary patterns are given to the circuit by using 15 input voltage supplies.

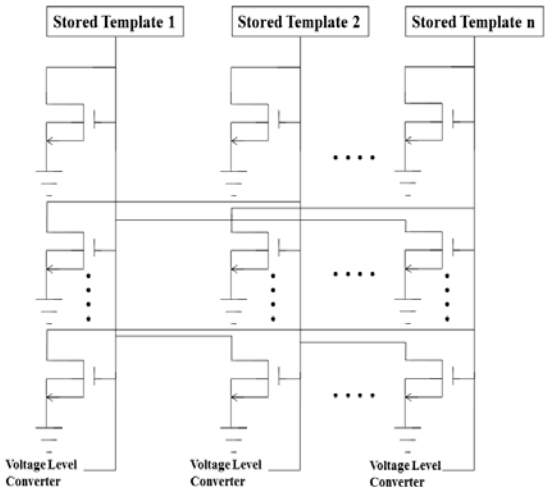


**Fig. 5: Winner take all circuit for N templates.**

Current generated at the output of particular neuron is proportional to the hamming distance of input and the stored pattern of the neuron. These currents generated in the tails of neurons compete in winner take all circuitry as shown in Fig. 5. During the process of competition node having highest

current cause increment in the voltage of that particular node and results in decrement of other template competition nodes which inhibits the unmatched templates nodes and provides output corresponding to matched template.[7,5]

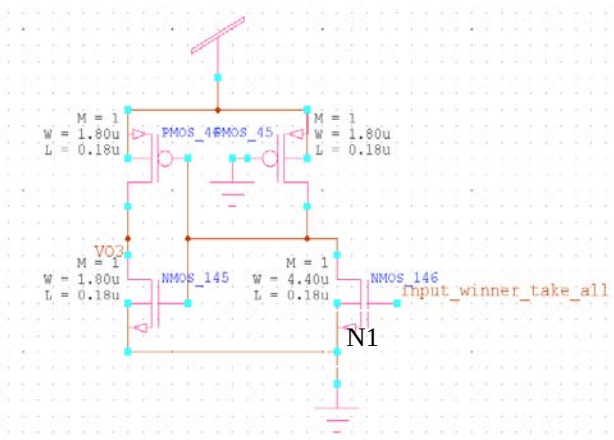


**Fig. 6: Voltage level converter.**

Voltages from different template competition nodes causes N1 transistor turned on or off which in turn generates high/low output voltage.

## 3. SIMULATION RESULT

The switched current hamming neural network provides output corresponding to closest match.

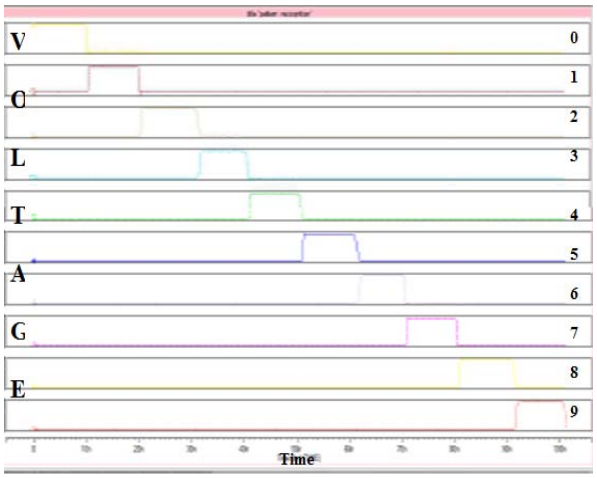


**Fig. 7: Transient simulation results for 0-9 digits pattern recognition.**

**Table 2: Rise time and fall time in ps.**

| Output Node | Rise Time | Fall Time |
|---|---|---|
| Vo0 | 513.83ps | 222.73ps |
| Vo1 | 158.91ps | 154.8ps |
| Vo2 | 235.1ps | 356.83ps |
| Vo3 | 145.87ps | 160.04ps |
| Vo4 | 257.65ps | 487.43ps |
| Vo5 | 349.36ps | 434.41ps |
| Vo6 | 692.04ps | 146.4ps |
| Vo7 | 309.35ps | 204.38ps |
| Vo8 | 377.08ps | 189.51ps |
| Vo9 | 662.52ps | 559.1ps |

Table 2 shows the rise time and fall time for the recognition of 0 to 9 digits pattern. Average propagation delay for each pattern can be determined by using equation given below.

$$\text{average propogation delay} = \frac{(\text{rise time} + \text{fall time})}{2}$$

From the simulation results total power consumption is 27.2mW

## 4. PROPOSED WORK

In this paper 0 to 9 digits pattern recognition neural network has been implemented [5]. Numbers of transistors are significant in this design if this circuit tried to extend for more patterns then there would be increment in number of transistors also. So in further work number of transistors would try to reduce with more efficient and precise results.

## 5. CONCLUSION

By using NMOS and PMOS topologies 0 to 9 digits are stored in different templates. These templates are being compared with input pattern. Current produce by all templates compete in winner take all circuits. Highest current will be generated by eventually highly matched pattern. This current will be converted in corresponding voltage level.

## 6. ACKNOWLEDGEMENTS

To analyze and to represent something new is the endeavor on a path towards an unmapped destination is a laborious quest unless one gets a proper guidance to show the way. The enlightening supervision, we found in our guide Mr. Krishan Verma, Chief Technology Officer, Silicon Mentor, Greater Noida, whose cooperation proves worthy to give final outline to this project.

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